CMP — Compare — CMP

Operation: (ACCX) – (M)

Description: Compares the contents of ACCX to the contents of M and sets the condition codes, which may be used for arithmetic and logical conditional branching. Both operands are unaffected.

Condition Codes and Boolean Formulae:

S	X	H	I	N	Z	V	C
—	—	—	—	⇕	⇕	⇕	⇕

N R7
Set if MSB of result is set; cleared otherwise.

Z $\overline{R7} \cdot \overline{R6} \cdot \overline{R5} \cdot \overline{R4} \cdot \overline{R3} \cdot \overline{R2} \cdot \overline{R1} \cdot \overline{R0}$
Set if result is $00; cleared otherwise.

V $X7 \cdot \overline{M7} \cdot \overline{R7} + \overline{X7} \cdot M7 \cdot R7$
Set if a twos complement overflow resulted from the operation; cleared otherwise.

C $\overline{X7} \cdot M7 + M7 \cdot R7 + R7 \cdot \overline{X7}$
Set if there was a borrow from the MSB of the result; cleared otherwise.

Source Forms: CMPA (opr); CMPB (opr)

Addressing Modes, Machine Code, and Cycle-by-Cycle Execution:

Cycle	CMPA (IMM)			CMPA (DIR)			CMPA (EXT)			CMPA (IND,X)			CMPA (IND,Y)		
	Addr	Data	R/W	Addr	Data	R/W	Addr	Data	R/W	Addr	Data	R/W	Addr	Data	R/W
1	OP	81	1	OP	91	1	OP	B1	1	OP	A1	1	OP	18	1
2	OP + 1	ii	1	OP + 1	dd	1	OP + 1	hh	1	OP + 1	ff	1	OP + 1	A1	1
3				00dd	(00dd)	1	OP + 2	ll	1	FFFF	—	1	OP + 2	ff	1
4							hhll	(hhll)	1	X + ff	(X + ff)	1	FFFF	—	1
5													Y + ff	(Y + ff)	1

Cycle	CMPB (IMM)			CMPB (DIR)			CMPB (EXT)			CMPB (IND,X)			CMPB (IND,Y)		
	Addr	Data	R/W	Addr	Data	R/W	Addr	Data	R/W	Addr	Data	R/W	Addr	Data	R/W
1	OP	C1	1	OP	D1	1	OP	F1	1	OP	E1	1	OP	18	1
2	OP + 1	ii	1	OP + 1	dd	1	OP + 1	hh	1	OP + 1	ff	1	OP + 1	E1	1
3				00dd	(00dd)	1	OP + 2	ll	1	FFFF	—	1	OP + 2	ff	1
4							hhll	(hhll)	1	X + ff	(X + ff)	1	FFFF	—	1
5													Y + ff	(Y + ff)	1

BRA — Branch Always — BRA

Operation: PC ⇐ (PC) + $0002 + Rel

Description: Unconditional branch to the address given by the foregoing formula, in which Rel is the relative offset stored as a twos-complement number in the second byte of machine code corresponding to the branch instruction.

The source program specifies the destination of any branch instruction by its absolute address, either as a numerical value or as a symbol or expression, that can be numerically evaluated by the assembler. The assembler obtains the relative address, Rel, from the absolute address and the current value of the location counter.

Condition Codes and Boolean Formulae:

S	X	H	I	N	Z	V	C
—	—	—	—	—	—	—	—

None affected

Source Form: BRA (rel)

Addressing Modes, Machine Code, and Cycle-by-Cycle Execution:

Cycle	BRA (REL)		
	Addr	Data	R/W
1	OP	20	1
2	OP + 1	rr	1
3	FFFF	—	1

The following table is a summary of all branch instructions.

Test	Boolean	Mnemonic	Opcode	Complementary		Branch	Comment
r > m	Z + (N ⊕ V) = 0	BGT	2E	r ≤ m	BLE	2F	Signed
r ≥ m	N ⊕ V = 0	BGE	2C	r < m	BLT	2D	Signed
r = m	Z = 1	BEQ	27	r ≠ m	BNE	26	Signed
r ≤ m	Z + (N ⊕ V) = 1	BLE	2F	r > m	BGT	2E	Signed
r < m	N ⊕ V = 1	BLT	2D	r ≥ m	BGE	2C	Signed
r > m	C + Z = 0	BHI	22	r ≤ m	BLS	23	Unsigned
r ≥ m	C = 0	BHS/BCC	24	r < m	BLO/BCS	25	Unsigned
r = m	Z = 1	BEQ	27	r ≠ m	BNE	26	Unsigned
r ≤ m	C + Z = 1	BLS	23	r > m	BHI	22	Unsigned
r < m	C = 1	BLO/BCS	25	r ≥ m	BHS/BCC	24	Unsigned
Carry	C = 1	BCS	25	No Carry	BCC	24	Simple
Negative	N = 1	BMI	2B	Plus	BPL	2A	Simple
Overflow	V = 1	BVS	29	No Overflow	BVC	28	Simple
r = 0	Z = 1	BEQ	27	r ≠ 0	BNE	26	Simple
Always	—	BRA	20	Never	BRN	21	Unconditional