LDA — Load Accumulator — LDA

Operation: ACCX ⇐ (M)

Description: Loads the contents of memory into the 8-bit accumulator. The condition codes are set according to the data.

Condition Codes and Boolean Formulae:

S	X	H	I	N	Z	V	C
—	—	—	—	⇕	⇕	0	—

N R7
Set if MSB of result is set; cleared otherwise.
Z $\overline{R7} \cdot \overline{R6} \cdot \overline{R5} \cdot \overline{R4} \cdot \overline{R3} \cdot \overline{R2} \cdot \overline{R1} \cdot \overline{R0}$
Set if result is $00; cleared otherwise.
V 0
Cleared

Source Forms: LDAA (opr); LDAB (opr)

Addressing Modes, Machine Code, and Cycle-by-Cycle Execution:

Cycle	LDAA (IMM)			LDAA (DIR)			LDAA (EXT)			LDAA (IND,X)			LDAA (IND,Y)		
	Addr	Data	R/W	Addr	Data	R/W	Addr	Data	R/W	Addr	Data	R/W	Addr	Data	R/W
1	OP	86	1	OP	96	1	OP	B6	1	OP	A6	1	OP	18	1
2	OP + 1	ii	1	OP + 1	dd	1	OP + 1	hh	1	OP + 1	ff	1	OP + 1	A6	1
3				00dd	(00dd)	1	OP + 2	ll	1	FFFF	—	1	OP + 2	ff	1
4							hhll	(hhll)	1	X + ff	(X + ff)	1	FFFF	—	1
5													Y + ff	(Y + ff)	1

Cycle	LDAB (IMM)			LDAB (DIR)			LDAB (EXT)			LDAB (IND,X)			LDAB (IND,Y)		
	Addr	Data	R/W	Addr	Data	R/W	Addr	Data	R/W	Addr	Data	R/W	Addr	Data	R/W
1	OP	C6	1	OP	D6	1	OP	F6	1	OP	E6	1	OP	18	1
2	OP + 1	ii	1	OP + 1	dd	1	OP + 1	hh	1	OP + 1	ff	1	OP + 1	E6	1
3				00dd	(00dd)	1	OP + 2	ll	1	FFFF	—	1	OP + 2	ff	1
4							hhll	(hhll)	1	X + ff	(X + ff)	1	FFFF	—	1
5													Y + ff	(Y + ff)	1

STA — Store Accumulator — STA

Operation: M ⇐ (ACCX)

Description: Stores the contents of ACCX in memory. The contents of ACCX remain the same.

Condition Codes and Boolean Formulae:

S	X	H	I	N	Z	V	C
—	—	—	—	⇕	⇕	0	—

N X7
Set if MSB of result is set; cleared otherwise.
Z $\overline{X7} \cdot \overline{X6} \cdot \overline{X5} \cdot \overline{X4} \cdot \overline{X3} \cdot \overline{X2} \cdot \overline{X1} \cdot \overline{X0}$
Set if result is $00; cleared otherwise.
V 0
Cleared

Source Forms: STAA (opr); STAB (opr)

Addressing Modes, Machine Code, and Cycle-by-Cycle Execution:

Cycle	STAA (DIR)			STAA (EXT)			STAA (IND,X)			STAA (IND,Y)		
	Addr	Data	R/W	Addr	Data	R/W	Addr	Data	R/W	Addr	Data	R/W
1	OP	97	1	OP	B7	1	OP	A7	1	OP	18	1
2	OP + 1	dd	1	OP + 1	hh	1	OP + 1	ff	1	OP + 1	A7	1
3	00dd	(A)	0	OP + 2	ll	1	FFFF	—	1	OP + 2	ff	1
4				hhll	(A)	0	X + ff	(A)	0	FFFF	—	1
5										Y + ff	(A)	0

Cycle	STAB (DIR)			STAB (EXT)			STAB (IND,X)			STAB (IND,Y)		
	Addr	Data	R/W	Addr	Data	R/W	Addr	Data	R/W	Addr	Data	R/W
1	OP	D7	1	OP	F7	1	OP	E7	1	OP	18	1
2	OP + 1	dd	1	OP + 1	hh	1	OP + 1	ff	1	OP + 1	E7	1
3	00dd	(B)	0	OP + 2	ll	1	FFFF	—	1	OP + 2	ff	1
4				hhll	(B)	0	X + ff	(B)	0	FFFF	—	1
5										Y + ff	(B)	0

ADD — Add without Carry — ADD

Operation: ACCX ⇐ (ACCX) + (M)

Description: Adds the contents of M to the contents of ACCX and places the result in ACCX. This instruction affects the H condition code bit so it is suitable for use in BCD arithmetic operations (see DAA instruction for additional information).

Condition Codes and Boolean Formulae:

S	X	H	I	N	Z	V	C
—	—	⇕	—	⇕	⇕	⇕	⇕

H $X3 \cdot M3 + M3 \cdot \overline{R3} + \overline{R3} \cdot X3$
Set if there was a carry from bit 3; cleared otherwise.

N R7
Set if MSB of result is set; cleared otherwise.

Z $\overline{R7} \cdot \overline{R6} \cdot \overline{R5} \cdot \overline{R4} \cdot \overline{R3} \cdot \overline{R2} \cdot \overline{R1} \cdot \overline{R0}$
Set if result is $00; cleared otherwise.

V $X7 \cdot M7 \cdot \overline{R7} + \overline{X7} \cdot \overline{M7} \cdot R7$
Set if a twos complement overflow resulted from the operation; cleared otherwise.

C $X7 \cdot M7 + M7 \cdot \overline{R7} + \overline{R7} \cdot X7$
Set if there was a carry from the MSB of the result; cleared otherwise.

Source Forms: ADDA (opr); ADDB (opr)

Addressing Modes, Machine Code, and Cycle-by-Cycle Execution:

Cycle	ADDA (IMM)			ADDA (DIR)			ADDA (EXT)			ADDA (IND,X)			ADDA (IND,Y)		
	Addr	Data	R/W	Addr	Data	R/W	Addr	Data	R/W	Addr	Data	R/W	Addr	Data	R/W
1	OP	8B	1	OP	9B	1	OP	BB	1	OP	AB	1	OP	18	1
2	OP + 1	ii	1	OP + 1	dd	1	OP + 1	hh	1	OP + 1	ff	1	OP + 1	AB	1
3				00dd	(00dd)	1	OP + 2	ll	1	FFFF	—	1	OP + 2	ff	1
4							hhll	(hhll)	1	X + ff	(X + ff)	1	FFFF	—	1
5													Y + ff	(Y + ff)	1

Cycle	ADDB (IMM)			ADDB (DIR)			ADDB (EXT)			ADDB (IND,X)			ADDB (IND,Y)		
	Addr	Data	R/W	Addr	Data	R/W	Addr	Data	R/W	Addr	Data	R/W	Addr	Data	R/W
1	OP	CB	1	OP	DB	1	OP	FB	1	OP	EB	1	OP	18	1
2	OP + 1	ii	1	OP + 1	dd	1	OP + 1	hh	1	OP + 1	ff	1	OP + 1	EB	1
3				00dd	(00dd)	1	OP + 2	ll	1	FFFF	—	1	OP + 2	ff	1
4							hhll	(hhll)	1	X + ff	(X + ff)	1	FFFF	—	1
5													Y + ff	(Y + ff)	1